R E M A R K S

Careful review and examination of the subject application are noted and appreciated. Applicants' representative thanks Examiner Trujillo for the indication of allowable subject matter.

SUPPORT FOR CLAIM AMENDMENTS

Support for the amendments to the claims can be found in the drawings as originally filed, for example, on FIGS. 2-4 and in the specification as original filed, for example, on page 12, lines 3-10 and on page 15, line 1 through page 16, line 9. As such, no new matter has been introduced.

CLAIM REJECTIONS UNDER 35 U.S.C. §112

The rejection of claims 16 and 17 under 35 U.S.C. §112, second paragraph, has been obviated by appropriate amendment and should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §102

The rejection of claims 1, 2, 7, 8, 14 and 18-20 under 35 U.S.C. §102 as being anticipated by Poisner et al. (U.S. Patent No. 6,269,443; hereinafter Poisner) has been obviated by appropriate amendment and should be withdrawn.

Poisner is directed to method and apparatus for automatically selecting a CPU clock frequency multiplier.

In contrast, the present invention (claim 1) provides a first circuit configured to generate a plurality of first clock signals, each having a frequency determined in response to one or more first control signals. Claims 18 and 19 include similar limitations. Poisner does not disclose or suggest each and every element of the presently claimed invention, arranged as in the claims. As such, the presently claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

Specifically, Poisner teaches selecting **a clock frequency multiplier for a CPU** (column 1, lines 6-8 and column 2, lines 10-12 and 42-43 of Poisner). Poisner appears silent regarding generating **a plurality of clock signals, each having a frequency determined in response to one or more first control signals**, as presently claimed. Therefore, Poisner does not disclose or suggest each and every element of the presently claimed invention, arranged as in the claims. As such, the presently claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

With respect to claims 16 and 17, claim 16 has been rewritten in independent form and amended as suggested on page 13, paragraph no. 34 of the Office Action. Therefore, claim 16 is believed to be allowable. Claim 17 depends directly from claim 16 which is believed to be allowable. As such, the presently claimed

invention is fully patentable over the cited reference and the rejection should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §103

The rejection of claims 3, 4, 19 and 20 under 35 U.S.C. §103(a) as being unpatentable over Poisner in view of Mote, Jr. (U.S. Patent No. 5,630,110; hereinafter Mote) has been obviated by appropriate amendment and should be withdrawn.

The rejection of claims 5 and 16 under 35 U.S.C. §103(a) as being unpatentable over Poisner in view of Gupta et al. (U.S. Patent No. 5,996,083; hereinafter Gupta) has been obviated by appropriate amendment and should be withdrawn.

The rejection of claims 6 and 9-13 under 35 U.S.C. §103(a) as being unpatentable over Poisner in view of Allen et al. (U.S. Patent No. 5,233,613; hereinafter Allen) has been obviated by appropriate amendment and should be withdrawn.

The rejection of claim 15 under 35 U.S.C. §103(a) as being unpatentable over Poisner in view of the 1^2C Bus Specification has been obviated by appropriate amendment and should be withdrawn.

The rejection of claim 21 under 35 U.S.C. §103(a) as being unpatentable over Poisner in view of Finch et al. (U.S. Patent No. 5,513,319; hereinafter Finch) has been obviated by appropriate amendment and should be withdrawn.

Mote is directed to a method and apparatus for enhancing performance of a processor (Title of Mote). Gupta is directed to

a microprocessor having software controllable power consumption (Title of Gupta). Allen is directed to a reliable watchdog timer (Title of Allen).

For the reasons presented above, Poisner does not teach or suggest each and every element of the presently pending claims 1, 18 and 19. Specifically, Poisner does not teach or suggest a first circuit configured to generate **a plurality of first clock signals, each having a frequency determined in response to one or more first control signals**, as presently claimed.

Mote and Gupta do not appear to cure the deficiencies of Poisner. In particular, Mote and Gupta appear to be silent regarding a first circuit configured to **generate a plurality of first clock signals**, each having a frequency determined in response to one or more first control signals, as presently claimed. Therefore, Poisner, Mote and Gupta, alone or in combination, do not teach or suggest each and every element of the presently claimed invention. As such, the presently claimed invention is fully patentable over the cited references and the rejections should be withdrawn.

Allen also does not cure the deficiencies of Poisner. Allen appears to be silent regarding a first circuit configured to generate a plurality of first clock signals, **each having a frequency determined in response to one or more first control signals** and **a second circuit configured to generate the one or more first control signals and a second control signal in response to a**

data signal and a second clock signal, as presently claimed. Specifically, assuming, *arguendo*, the signal CLKS in FIG. 1 of Allen is similar to the presently claimed plurality of first clock signals, and the signal CNTL of Allen is similar to the presently claimed one or more first control signals (for which Applicants' representative does not necessarily agree), Allen appears silent regarding a circuit configured to generate a plurality of first clock signals, each having a frequency determined in response to one or more first control signals or a circuit configured to generate the one or more first control signals in response to a data signal and a second clock signal, as presently claimed.

In particular, with respect to the signals CLKS and CNTL in Allen states:

> FIG. 1 is a block diagram of a processor employing the present invention. The processor includes a CPU 100 that performs standard microcontroller or microcomputer processes under program control. In addition, a system clock 101 generates clock signals CLKS on lines 102 and 103 for supply throughout the system. The CPU 100 in the preferred embodiment, is a data processor operating with a six-state instruction cycle and a two-phase clock. This system clock feature is reflected in the detailed implementation set out below with reference to FIGS. 2-9. The CPU 100 and system clock 101 communicate control information CNTL across line 104.
>
> The processor of FIG. 1 includes a watchdog timer 105 according to the present invention. The watchdog timer 105 receives system clocks across line 102 and communicates control information CNTL with the CPU 100 across line 106. In addition, a bus 107 is provided for communicating data between the CPU 100 and the watchdog timer 105 in response to the control

information CNTL on line 106 (column 3, lines 6-26 of Allen).

Nowhere in the above text does Allen appear to teach or suggest that the signal CLKS has a frequency determined in response to the signal CNTL or that the signal CNTL is generated in response to a data signal and a second clock signal, as presently claimed. Furthermore, a search of the Allen reference for the word "frequency" or "frequencies" found no occurrences. Therefore, Poisner and Allen, alone or in combination, do not teach or suggest each and every element of the presently claimed invention. As such, the presently claimed invention is fully patentable over the cited references and the rejection should be withdrawn.

With respect to claims 16 and 17, claim 16 has been rewritten in independent form and amended as suggested on page 13, paragraph no. 34 of the Office Action. Therefore, claim 16 is believed to be allowable over the cited references. Claim 17 depends directly from claim 16 which is believed to be allowable. As such, the presently claimed invention is fully patentable over the cited references and the rejections should be withdrawn.

Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge our office Account No. 50-0541.

Respectfully submitted,

CHRISTOPHER P. MAIORANA, P.C.

Robert M. Miller
Registration No. 42,892
24840 Harper Avenue, Suite 100
St. Clair Shores, MI 48080
(586) 498-0670

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